REMARKS

Claims 1-3 and 6-11 are pending, claims 4-5 have previously been canceled, and claims 12-34 have previously been withdrawn. Pending claims 1-3 and 6-11 stand rejected. No amendments to the claims are currently presented.

Claims 1-3 and 10-11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,754,116 ("Janik") in view of U.S. Patent No. 5,287,470 ("Simpson"), and claims 6-9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Janik in view of Simpson and further in view of U.S. Patent No. 6,430,648 ("Carnevale").

Applicants respectfully traverse because the combination of Janik and Simpson does not disclose the invention recited in sole independent claim 1 for at least two reasons. First, claim 1 recites that the muxing device circuit is configurable so that the first memory access device is coupled to the first memory bank and the second memory access device is discretely and simultaneously coupled to the second memory device. Even assuming that Simpson discloses simultaneous coupling to two memory devices, Janik does not disclose two discrete connections because the processor 3, which generates multi-bank commands (i.e., commands that access a plurality of memory banks simultaneously) and the BIST 2, which generates single-bank commands, both access the same memory bank at the same time.

For example, with reference to Figure 2 of Janik, if the BIST 2 generates a single-bank command I to memory bank A, and the processor 3 generates a multi-bank command II to memory banks A and B, and the BIST and processor are given simultaneous access to the memory banks A and B according to Simpson, then both the BIST and the processor will be connected to memory bank A at the same time. Thus, the combination of Janik and Simpson does not disclose discrete couplings between memory access devices and respective memory banks because two memory access devices access the same memory device at the same time.

Second, claim 1 recites that the data transmitted to the memory devices is non-interleaved, but both Janik and Simpson disclose the transmission of interleaved data. Janik

discusses that in the prior art, testing circuits were unable to access more than one memory bank in a given clock cycle. *See* Janik at col. 2, ll. 24-42. As such, commands for testing memory bank A would be transmitted prior to transmitting commands for testing memory bank B. *See id.* at col. 8, ll. 18-21; Fig. 3A. Janik overcame this problem by disclosing a processor 3 that interleaves a plurality of commands to memory bank A with a plurality of commands to memory bank B so that in a given clock cycle, one single-bank command to each memory bank (packaged as a multi-bank command) is transmitted to the multi-bank memory for simultaneous execution by both memory banks. *See id.* at col. 3, ll. 23-46; Fig. 3B. Janik therefore teaches transmitting interleaved data to the multi-bank memory.

Similarly, Figures 10 and 11 in Simpson disclose two interleaved memory banks 300, 302 that are configured to store alternate 32-bit pixel words. *See* Simpson at col. 9, ll. 23-31. Simpson discloses that pixel data to be stored in memory bank0 is interleaved with the pixel data to be stored in memory bank1 such that words 0, 2, etc., are stored to bank0 and words 1, 3, etc., are stored to bank1. *See id.* at col. 9, ll. 29-36. Thus, assuming that two memory access devices were transmitting data to two interleaved memory banks in Simpson's apparatus, Simpson requires interleaving the data so that both memory banks may receive data simultaneously.

Applicants have responded to all of the rejections recited in the Office Action. Reconsideration and a Notice of Allowance for claims 1-3 and 6-11 is therefore respectfully requested.

In view of the above, claims 1-3 and 6-11 are believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

If the Examiner believes an interview would be of assistance, the Examiner is welcome to contact the undersigned at the number listed below.

In the event a fee is required or if any additional fee during the prosecution of this application is not paid, the Patent Office is authorized to charge the underpayment to Deposit Account No. 50-2215.

Dated: February 26, 2008

Respectfully submitted,

By _____

Peter Lambrianakos
Registration No.: 58,279
DICKSTEIN SHAPIRO LLP
1177 Avenue of the Americas
New York, New York 10036-2714
(212) 277-6500
Attorney for Applicant